ABSTRACT

The disclosure includes a description of a content addressable memory (CAM) that includes at least one tag input, at least one output, and at least one random access memory. The CAM includes circuitry to perform multiple read operations of the at least one random access memory with different ones of the read operations specifying an address being based on different subsets of tag bits. Based on the multiple read operations, the CAM generates at least one signal via the at least one output.